**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Applicants: | Pradeep Sindhu; Dennis C. Ferguson | Confirmation No. | 4412 |
| Serial No.: | 10/004,536 | | |
| Filed: | October 31, 2001 | Customer No.: | 28863 |
| Examiner: | Joseph E. Avellino | | |
| Group Art Unit: | 2143 | | |
| Docket No.: | 1014-014US01/JNP-0074 | | |
| Title: | NETWORK ROUTER HAVING EMBEDDED MEMORY | | |

**SUPPLEMENTAL REPLY BRIEF**

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This is a Supplemental Reply Brief filed in response to an Office Communication (Paper 20070521) mailed May 24, 2007. Appellant submits this Supplemental Reply Brief because in the Office Communication the Examiner raised a new rationale for the rejection, thus necessitating this Supplemental Reply Brief.

No fee is believed due. Please charge any deficiencies or credits to Deposit Account No. 50-1778.

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## REAL PARTY IN INTEREST

The real party in interest is Juniper Networks, Inc. of Sunnyvale, California.

## RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

## STATUS OF CLAIMS

Claims 1-9, 11-20, 22-26, 28-32 and 34-35 are on appeal in this case. All claims are being appealed.

All claims stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

In the Examiner's Answer, the Examiner raised a new ground of rejection and rejected all claims under 35 U.S.C. 102(c) as being anticipated by Bass et. al (USPN 6,460,120).

## STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed June 16, 2006 from which this Appeal has been made.

## SUMMARY OF THE CLAIMED SUBJECT MATTER

A concise summary of independent claims 1, 9, 18, 24, 30 and 35 is provided within Appellant's Brief filed December. Per MPEP 1208, the Summary of the Claimed Subject Matter has been omitted from this Reply Brief.

## GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The first grounds for rejection to be reviewed on Appeal is the rejection of claims 1-9, 11-20, 22-26, 28-32 and 34-35 under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

2. The second grounds for rejection to be reviewed on Appeal is the rejection of claims 1-9, 11-20, 22-26, 28-32 and 34-35 under 35 U.S.C. 102(e) as being anticipated by Bass et al. (USPN 6,460,120).

## SUPPLEMENTAL ARGUMENTS

*Response to the Office Communication Mailed May 24, 2007*

In this Supplemental Reply Brief, Appellant addresses only the arguments presented by the Examiner in the recent Office Communication mailed May 24, 2007. In the Office Communication, the Examiner raised a new rationale as a basis for maintaining the rejection.

In the Office Communication the Examiner addressed the limitations of claim 1 that require a routing component having a control unit that received data from a network using a first interface and, based on the destination of the data: (i) buffers data using embedded memory internal to an integrated circuit when the destination requires forwarding the data to the second routing component of a router using a switch, and (ii) buffers the data in external memory when the destination requires forwarding the data to the network via the first interface. Specifically, the Examiner argued as follows:

> Irregardless [sic] of the claimed limitation, the second limitation does not necessarily have to occur in order to meet the claim. The packet is buffered in the external memory only "when the destination requires forwarding of the data to the network via the first interface", however since the packet received from the first interface only goes to the second interface (and to another routing component), this limitation does not occur, since the packet is buffered in internal memory "when the destination requires forwarding of the data to the second routing component."

Thus, the Examiner admits that the prior art of record does not contemplate forwarding the inbound packet back to the network by that interface without requiring the packet be forwarded to another routing component. He nevertheless argues that the prior meets the limitations of claim 1 simply because such a condition never arises with the particular structure of the prior art router.

Consequently, the Examiner erroneously overlooks the fact that claim 1 requires a routing component that includes a control unit having specific structural limitations and capabilities of determining a destination of a packet and (i) buffering data of that packet using the embedded memory internal to the integrated circuit when the destination

requires forwarding the data to the second routing component of the router using the switch, and (ii) buffering the data in the external memory when the destination requires forwarding the data to the network via the first interface. That is, claim 1 literally requires a controller *capable of buffering the data as recited by the claim upon determining that such packets are received.* By the Examiner's own admission the cited prior art does not even contemplate or in any way check for such a condition (all packets from one interface are sent to another routing component). The prior art clearly fails to describe a routing component including a control unit having the features recited in claim 1 for actively buffering the data differently in such situations. The fact that the prior art does not contemplate the situation, and therefore does not teach any such routing component or control unit capable of handling the situation, cannot be used as the basis for rejecting of Appellant's claims by effectively reading out limitations of the claims.

Appellant refers the Board to its previous Appeal Brief and Reply Brief in which the Appellant explains in detail that the literal language of claim 1 requires a routing component in which data received from the network on the same interface (e.g., inbound packets from WAN interface 14) are buffered differently by using either embedded memory or external memory based on the particular destination to which the data is to be forwarded. These arguments are incorporated herein by reference. Such claimed features are not taught or suggested by the prior art.

**Conclusion of Arguments**

The Examiner's new basis for maintaining the rejection as set forth in the recent Office Communication mailed May 24, 2007 is flawed. The Examiner erred in reading out claim elements based on a premise that the prior art does not contemplate certain conditions set forth in the claims. The Examiner erred in rejecting Appellant's claims under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680). The Examiner also erred in the rejection of claims 1-9, 11-20, 22-26, 28-32 and 34-35 rejected under 35 U.S.C. 102(e) as being anticipated by Bass et al. (USPN 6,460,120).

Reversal of the rejections and allowance of the pending claims are requested.

Respectfully submitted,

Date: June 26, 2007

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## APPENDIX: CLAIMS ON APPEAL

Claim 1 (Previously Presented): A routing component of a router comprising:

a first interface to communicate data with a network;

a second interface to communicate data to a second routing component using a switch internal to the router, wherein the first interface and the second interface are integrated within a single integrated circuit;

an embedded memory within the integrated circuit;

a memory interface to couple the integrated circuit to an external memory; and

at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data;

wherein the control unit buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

Claim 2 (Previously Presented): The routing component of claim 1, wherein the at least one control unit comprises:

a first control unit to buffer in the embedded memory data that is received from the first interface and forwarded to the second interface; and

a second control unit to buffer in the external memory data that is received from the second interface and forwarded to the first interface.

Claim 3 (Original): The routing component of claim 2, wherein the external memory has a greater storage capacity than the embedded memory.

Claim 4 (Original): The routing component of claim 1, wherein the first interface comprises a wide area network (WAN) interface.

Claim 5 (Original): The routing component of claim 1, wherein the second interface comprises a switch fabric interface.

Claim 6 (Original): The routing component of claim 5, wherein the switch fabric interface communicates crossbar data.

Claim 7 (Previously Presented): The routing component of claim 1, wherein the routing component is implemented using a single application specific integrated circuit (ASIC).

Claim 8 (Original): The routing component of claim 1, wherein the embedded memory comprises a random access memory (RAM).

Claim 9 (Previously Presented): A network element comprising:

a first network interface to communicate data with a network;

a second network interface to communicate data with the network;

a routing component formed in an integrated circuit, wherein the routing component has an embedded memory within the integrated circuit; and

a second memory external to the routing component,

wherein the routing component receives data from the first network interface and accesses a forwarding table to determine a network destination for the data,

wherein the routing component buffers data in the embedded memory internal to the routing component when the destination requires forwarding the data to a second routing component using a switch internal to the network element, and

wherein the routing component buffers data communicated in the second memory external to the routing component when the destination requires forwarding the data to the network via the first network interface.

Claim 10 (Cancelled).

Claim 11 (Previously Presented): The network element of claim 9, wherein the second memory has a greater storage capacity than the embedded memory.

Claim 12 (Previously Presented): The network element of claim 9, wherein the first network interface and the second network interface comprise wide area network (WAN) interfaces.

Claim 13 (Previously Presented): The network element of claim 9, further comprising a crossbar switch fabric coupling the routing component to a second routing component.

Claim 14 (Previously Presented): The network element of claim 13, wherein the switch fabric communicates crossbar data.

Claim 15 (Previously Presented): The network element of claim 9, wherein the routing component is implemented using an application specific integrated circuit (ASIC).

Claim 16 (Original): The network element of claim 9, wherein the embedded memory comprises a random access memory (RAM).

Claim 17 (Previously Presented): The network element of claim 9, wherein the second routing component includes an embedded memory to store data communicated using the second network interface.

Claim 18 (Previously Presented): An integrated circuit (IC) comprising:

a first interface to communicate data with a network at a first data rate;

a second interface to communicate data with a switch fabric at a second data rate higher than the first data rate;

an embedded memory internal to the IC;

an interface to a memory external to the IC; and

at least one control unit that receives data from the first interface and accesses a forwarding table to determine a network destination for the data,

wherein the control unit buffers data in the embedded memory internal to the integrated circuit when the destination requires forwarding the data using the switch fabric, and

wherein the control unit buffers the data using the external memory when the destination requires forwarding the data out to the network via the first interface.

Claim 19 (Original): The IC of claim 18, wherein the memory external to the IC has a greater storage capacity than the embedded memory.

Claim 20 (Original): The IC of claim 18, wherein the first interface is coupled to a wide area network (WAN) interface.

Claim 21 (Cancelled).

Claim 22 (Previously Presented): The IC of claim 18, wherein the switch fabric comprises a crossbar.

Claim 23 (Original): The IC of claim 18, wherein the embedded memory comprises a random access memory (RAM).

Claim 24 (Previously Presented): A router comprising:

an integrated circuit (IC) comprising:

a first interface to communicate data with a network;

a second interface to communicate data with a switch fabric internal to the router;

an embedded memory; and

an interface to a memory external to the IC; and

at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data,

wherein the control unit buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to a routing component of the router using the switch fabric, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

Claim 25 (Original): The router of claim 24, wherein the memory external to the IC has a greater storage capacity than the embedded memory.

Claim 26 (Original): The router of claim 24, wherein the first interface is coupled to a wide area network (WAN) interface.

Claim 27 (Cancelled).

Claim 28 (Previously Presented): The router of claim 24, wherein the switch fabric comprises a crossbar.

Claim 29 (Original): The router of claim 24, wherein the embedded memory comprises a random access memory (RAM).

Claim 30 (Previously Presented): A method for communicating data using a network router, the method comprising:

receiving inbound data from a network interface via a first routing component;

accessing a forwarding table with a control unit of the network router to determine a network destination for the data;

when the destination requires forwarding the data to a second routing component internal to the router using a switch having a higher bandwidth than the network interface, buffering the inbound data within an embedded memory internal to the first routing component;

forwarding the inbound data from the first routing component to a second routing component via the switch;

receiving outbound data with the first routing component from the switch;

when the destination requires forwarding the outbound data to the network interface having a lower bandwidth than the switch, buffering the outbound data within a memory external to the first routing component; and

forwarding the outbound data to the network interface.

Claim 31 (Previously Presented): The method of claim 30, wherein the external memory has a greater storage capacity than the embedded memory.

Claim 32 (Previously Presented): The method of claim 30, wherein the first network interface comprises a wide area network (WAN) interface.

Claim 33 (Canceled).

Claim 34 (Previously Presented): The method of claim 30, wherein the switch communicates crossbar data.

Claim 35 (Previously Presented): A routing arrangement comprising:

a crossbar arrangement;

a plurality of routing components coupled to the crossbar arrangement, at least a first one of the routing components comprising:

a first interface to communicate data with a network;

a second interface to communicate data with the crossbar arrangement;

an embedded memory;

an external memory interface to a memory external to the routing component; and

at least one control unit that receives data from the first interface and determines a network destination for the data,

wherein the control unit buffers the data using the embedded memory internal to the routing component when the destination requires forwarding the data to a second one of the routing components using the crossbar arrangement, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

## APPENDIX: EVIDENCE

**None**

## APPENDIX: RELATED PROCEEDINGS

**None**